Synopsys Design Compiler User Guide

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Synopsys Design Compiler (DC) Basic Tutorial **Synopsys Design Compiler Synthesis Lecture (2013) COMPLETE ASIC SYNTHESIS ¦ SYNOPSYS ¦ DESIGN COMPILER (DESIGN VISION) ¦**

PHYSICAL DESIGN ¦ VLSIFaB S-5 ¦ Logic Synthesis of RTL in Synopsys Design Compiler ¦ RTL-to-GDSII flow ¦dc_shell ¦ DC Tutorial Synthesis in Synopsys Design Vision GUI tutorial Design synthesis using Synopsys Design Compiler

Logic Synthesis flow ¦ RTL Synthesis

flow ¦ RTL2GDS ¦ Design Compiler (DC) tutorialIntroducing Design Compiler NXT The Next-generation Design Compiler ¦ Synopsys ***Design Compiler NXT Faster, Better QoR and Advanced Node Ready ¦ Synopsys*** **Synopsys Tutorial Part 1 - Introduction to Synopsys Custom**

Designer Tools ***3 RTL Logic Synthesis Design Compiler Using Scripts Tutorial: Synthesis in Synopsys Design Vision and Place-and-Route in Cadence Encounter*** **Interview experience at Synopsys S-8 ¦ Physical Design Flow ¦ PnR flow ¦RTL-to-GDSII flow ¦ innovus tool flow Synopsys**

Tutorial Part 2 - Custom Designer Schematic Capture and HSpice Simulation Introduction to Floor planning What is Logic Synthesis? STATIC TIMING ANALYSIS ¦ SETUPP ¦ HOLD ¦ SYNOPSYS ¦ PRIMETIME ¦ PHYSICAL DESIGN ¦ VLSIFaB

S-9 ¦ Design Import ¦ Physical Design

¦RTL-to-GDSII flow ¦ Cadence innovus tutorial MACRO PLACEMENT ¦ FLOORPLAN ¦ CADENCE ¦ INNOVUS ¦ PHYSICAL DESIGN ¦ ASIC ¦ ELECTRONICS ¦ VLSIFaB ~~Timing Analysis using Prime Time~~ ~~Synopsys - IP/Hardware ¦ Synopsys~~ Synopsys VCS Basic tutorial - HDL simulation flow

Synopsys IC Compiler (ICC) basic tutorial **Synopsys Design Compiler installation** ~~**SDC file ¦ Synopsys Design Constraints file ¦ various files in VLSI Design ¦ session-4**~~ **Introduction to Synthesis** **ASIC DESIGN- LOGIC SYNTHESIS \u0026 PHYSICAL DESIGN USING SYNOPSYS DC AND ICC** **S-7 ¦**

Logic Equivalence Check using Formality ¦ RTL-to-GDSII flow ¦ Synopsys Formality tutorial How to Write a Literature Review: 3 Minute Step-by-step Guide ¦ Scribbr

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May 07, 2020 ^ Synopsys Ic Compiler User Guide ^ By Mary Higgins Clark, ic

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CS250 Tutorial 5 (Version 091210b) September 12, 2010 Yunsup Lee. In this tutorial you will gain experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library

as input and produces a gate-level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design.

~~RTL-to-Gates Synthesis using Synopsys Design Compiler~~

IC Compiler™ II Implementation User Guide, Version L-2016.03-SP4 ii ... This Synopsys software and all associ ated documentation are proprietary to Synopsys, Inc. and may only be used pursuant to the terms and conditions of a written license agreement with Synopsys, Inc. All other use,

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~~IC Compiler II Implementation User Guide~~

Execute the unified physical synthesis flow. Apply the power intent (UPF) Manage RTL-PG constructs. Enable

Incomplete UPF support. Apply a floorplan. Configure Fusion Compiler to create a floorplan on-the-fly. Perform MCMM setup: Define the corners, modes and scenarios required for. analysis and optimization.

~~Fusion Compiler Synthesis - Synopsys~~

Design Compiler NXT technology innovations include fast, highly efficient optimization engines, cloud-ready distributed synthesis, a new, highly accurate approach to RC estimation and capabilities required for the process nodes 5nm and below.

Download Datasheet. "We are collaborating with Synopsys on the latest synthesis technologies in Design Compiler NXT and are looking forward to deploying them on our designs to help meet our ever-increasing pressure of time-to-market and higher QoR."

~~Design Compiler NXT - Synopsys~~

The coreBuilder product is part of the complete set of IP reuse tools available from Synopsys. With coreBuilder, designers can easily capture all the components of an IP Core, including user configurable

design parameters in the core and set the boundaries and cross dependencies of these parameters. Users can also easily capture clock information, define the hierarchy of the core, and set constraints of the internal and external ports contained in the core.

~~coreBuilder | Synopsys~~

Design Compiler (Synopsys) Leonardo (Mentor Graphics) Front-End Design & Verification. Create Behavioral/RTL HDL Model(s) Simulate to Verify. Functionality. Synthesize. Circuit. Synopsys Design Compiler. Cadence

RTL Compiler. ... Define in file .synopsys_dc.setup DC User Guide. Chapter 4.

~~Automated Synthesis from HDL models~~

In this tutorial you will gain experience using Synopsys Design

Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and producesa gate-level netlist as output.

~~RTL-to-Gates Synthesis using~~

~~Synopsys Design Compiler~~

The Synopsys System Design Solutions (SDS) team brings 3 decades of experience and a vast first pass silicon track record built upon Synopsys ’ technology leadership. SDS works closely with customers to disrupt traditional design process,

enabling them to meet and exceed the most stringent requirements, driving next generation subsystem and SoC innovation beyond existing architectural limits.

~~System Design Solutions | Synopsys~~

Rtl Compiler User Guide For Flip Flop

In this tutorial you will use Synopsys Design Compiler to elaborate the RTL for our example greatest common divisor (GCD) cicruit, set optimization constraints, synthesize the design to gates, and prepare various area ... 4 Manual Design Compiler Build Process ... # to verify that latches and

flip-flops are not being accidentally inferred.

~~Rtl Compiler User Guide For Flip Flop~~| Synopsys maintains and runs an extensive suite of internal compiler verification and validation tests, and runs C and C++ validation suites from

Plum Hall, Inc. and Perennial, Inc. prior to every product release. The DesignWare ARC MetaWare C/C++ Debugger fully supports the rich set of ARC configuration options and extensions.

~~DesignWare ARC MetaWare~~

~~Development Toolkit | Synopsys~~

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced it intends to incorporate on-chip variation (OCV) extensions in

its open-source Liberty™ library format, the de-facto modeling standard for integrated circuit (IC) implementation and signoff.

~~Synopsys' Open-Source Liberty Format to Incorporate On ...~~

Synopsys® Timing Constraints and

Optimization User Guide Version D-2010.03, March 2010

~~Synopsys Timing Constraints and Optimization User Guide~~

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Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® Physical Compiler® and

PrimeTime®, Second Edition describes the advanced concepts and techniques used towards ASIC chip synthesis, physical synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM

(Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools, used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron

ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, physical synthesis, and static timing analysis. At each step, problems related to each phase of the design flow are

identified, with solutions and work-around described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the

basis of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solution. Target audiences for this book are practicing ASIC design engineers and masters level students undertaking advanced VLSI courses on ASIC chip design and DFT techniques.

Logic synthesis has become a fundamental component of the ASIC design flow, and Logic Synthesis Using Synopsys® has been written for all those who dislike reading manuals but who still like to learn logic synthesis as practised in the real

world. The primary focus of the book is Synopsys Design Compiler®: the leading synthesis tool in the EDA marketplace. The book is specially organized to assist designers accustomed to schematic capture based design to develop the required expertise to effectively use the

Compiler. Over 100 `classic scenarios' faced by designers using the Design Compiler have been captured and discussed, and solutions provided. The scenarios are based both on personal experiences and actual user queries. A general understanding of the problem-solving techniques

provided will help the reader debug similar and more complicated problems. Furthermore, several examples and dc-shell scripts are provided. Specifically, Logic Synthesis Using Synopsys® will help the reader develop a better understanding of the synthesis design flow,

optimization strategies using the Design Compiler, test insertion using the Test Compiler®, commonly used interface formats such as EDIF and SDF, and design re-use in a synthesis-based design methodology. Examples have been provided in both VHDL and Verilog. Audience: Written with

CAD engineers in mind to enable them to formulate an effective synthesis-based ASIC design methodology. Will also assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

After a brief introduction to low-power VLSI design, the design space of ASIP instruction set architectures (ISAs) is introduced with a special focus on important features for digital signal processing. Based on the degrees of freedom offered by

this design space, a consistent ASIP design flow is proposed: this design flow starts with a given application and uses incremental optimization of the ASIP hardware, of ASIP coprocessors and of the ASIP software by using a top-down approach and by applying application-specific

modifications on all levels of design hierarchy. A broad range of real-world signal processing applications serves as vehicle to illustrate each design decision and provides a hands-on approach to ASIP design. Finally, two complete case studies demonstrate the feasibility and the

efficiency of the proposed methodology and quantitatively evaluate the benefits of ASIPs in an industrial context.

Computing systems are undergoing a transformation from logic-centric towards memory-centric

architectures, where overall performance and energy efficiency at the system level are determined by the density, performance, functionality and efficiency of the memory, rather than the logic sub-system. This is driven by the requirements of data-intensive

applications in artificial intelligence, autonomous systems, and edge computing. We are at an exciting time in the semiconductor industry where several innovative device and technology concepts are being developed to respond to these demands, and capture shares of the

fast growing market for AI-related hardware. This special issue is devoted to highlighting, discussing and presenting the latest advancements in this area, drawing on the best work on emerging memory devices including magnetic, resistive, phase change, and other

types of memory. The special issue is interested in work that presents concepts, ideas, and recent progress ranging from materials, to memory devices, physics of switching mechanisms, circuits, and system applications, as well as progress in modeling and design tools.

Contributions that bridge across several of these layers are especially encouraged.

Field-programmable gate arrays (FPGAs), which are pre-fabricated, programmable digital integrated circuits (ICs), provide easy access to

state-of-the-art integrated circuit process technology, and in doing so, democratize this technology of our time. This book is about comparing the qualities of FPGA – their speed performance, area and power consumption, against custom-fabricated ICs, and exploring ways of

mitigating their de ciencies. This work began as a question that many have asked, and few had the resources to answer – how much worse is an FPGA compared to a custom-designed chip? As we dealt with that question, we found that it was far more dif cult to answer than we

anticipated, but that the results were rich basic insights on fundamental understandings of FPGA architecture. It also encouraged us to nd ways to leverage those insights to seek ways to make FPGA technology better, which is what the second half of the book is about. While the question

“How much worse is an FPGA than an ASIC?” has been a constant sub-theme of all research on FPGAs, it was posed most directly, some time around May 2004, by Professor Abbas El Gamal from Stanford University to us – he was working on a 3D FPGA, and was wondering if any real

measurements had been made in this kind of comparison. Shortly thereafter we took it up and tried to answer in a serious way.

This book describes novel software concepts to increase reliability under user-defined constraints. The

authors ' approach bridges, for the first time, the reliability gap between hardware and software. Readers will learn how to achieve increased soft error resilience on unreliable hardware, while exploiting the inherent error masking characteristics and error (stemming from soft errors,

aging, and process variations) mitigations potential at different software layers.

This book describes new and effective methodologies for modeling, analyzing and mitigating cell-internal signal electromigration in nanoCMOS,

with significant circuit lifetime improvements and no impact on performance, area and power. The authors are the first to analyze and propose a solution for the electromigration effects inside logic cells of a circuit. They show in this book that an interconnect inside a

cell can fail reducing considerably the circuit lifetime and they demonstrate a methodology to optimize the lifetime of circuits, by placing the output, Vdd and Vss pin of the cells in the less critical regions, where the electromigration effects are reduced. Readers will be enabled to apply this

methodology only for the critical cells in the circuit, avoiding impact in the circuit delay, area and performance, thus increasing the lifetime of the circuit without loss in other characteristics.

This book describes for readers a

methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling

(TLPM). Readers will benefit from this innovative way of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

Explains how to use low power design

in an automated design flow, and examine the design time and performance trade-offs Includes the latest tools and techniques for low power design applied in an ASIC design flow Focuses on low power in an automated design methodology, a much neglected area

Modern consumers carry many electronic devices, like a mobile phone, digital camera, GPS, PDA and an MP3 player. The functionality of each of these devices has gone through an important evolution over recent years, with a steep increase in

both the number of features as in the quality of the services that they provide. However, providing the required compute power to support (an uncompromised combination of) all this functionality is highly non-trivial. Designing processors that meet the demanding requirements of

future mobile devices requires the optimization of the embedded system in general and of the embedded processors in particular, as they should strike the correct balance between flexibility, energy efficiency and performance. In general, a designer will try to minimize the

energy consumption (as far as needed) for a given performance, with a sufficient flexibility. However, achieving this goal is already complex when looking at the processor in isolation, but, in reality, the processor is a single component in a more complex system. In order to design

such complex system successfully, critical decisions during the design of each individual component should take into account effect on the other parts, with a clear goal to move to a global Pareto optimum in the complete multi-dimensional exploration space. In the complex,

global design of battery-operated embedded systems, the focus of Ultra-Low Energy Domain-Specific Instruction-Set Processors is on the energy-aware architecture exploration of domain-specific instruction-set processors and the co-optimization of the datapath

architecture, foreground memory, and instruction memory organisation with a link to the required mapping techniques or compiler steps at the early stages of the design. By performing an extensive energy breakdown experiment for a complete embedded platform, both

energy and performance bottlenecks have been identified, together with the important relations between the different components. Based on this knowledge, architecture extensions are proposed for all the bottlenecks.